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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
|---|---|---|---|---|
| 10/763,089 | 01/22/2004 | Brian Barrick | AUS920030970US1 | 6064 |

50170 7590 03/22/2006

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| EXAMINER | |
|---|---|
| COLEMAN, ERIC | |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2183 | |

DATE MAILED: 03/22/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/763,089 | BARRICK, BRIAN | |
| | Examiner | Art Unit | |
| | Eric Coleman | 2183 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) 1-19 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-19 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## DETAILED ACTION

### *Claim Rejections - 35 USC § 102*

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

2. Claims 1,3-12,14-16,18,19 are rejected under 35 U.S.C. 102(a) as being anticipated by Fischer (patent No. 6,542,987) (As per claims 1,3,7,8,12,16):

Fischer taught the invention as claimed including a data processing ("DP") system comprising:

Performance logic, wherein the performance logic is at least configured to perform a plurality of commands issued by a processor, and wherein the performance logic further comprises a command queue with a predefined number of slots for storing the plurality of commands issued by the processor (e.g., see figs. 1,17A, 17B and col. 11,line 65-col. 12, line 8);

A command pipeline, wherein the command pipeline at least communicates the plurality of commands issued by the processor to the performance logic (e.g., see fig. 1);

A plurality of counters wherein the plurality of counters at least determine a known count of a number of commands in the command pipeline and in the command

queue, and wherein the plurality of counters at least predicts an unknown count further commands (e.g., see fig. 13); and

Stall logic (401), wherein the stall logic at least has the ability to stall performance of the plurality of commands issued by the processor based on at least a use of the unknown count and the unknown count (e.g., see col. 10, lines 1-46).

3. As to the known count (and counter therefore) (claims 1,3,7,8,14,18) Fisher determines the count of free slot plus the number of issued instructions , and then subtracts the number or instructions enqued in the present cycle plus the number of speculatively issued instructions that produce a cache hit. The count of the number of commands in the queue and pipeline does not particularize how these are used in the calculation. The count of instruction in the queue corresponds to the count of free slots as taught by Fisher. The number of total slots would have been set as a hardware limitation. The number of free slot would have been number of total slots minus the number of instructions in the queue no matter how many instructions were in the queue. The number of instruction in the pipeline would have been the number of issued instructions. Both the claimed invention and the Fisher system would have known this number as the count of issued instructions in the queue plus number of instructions executing comprises the number of instructions in the pipeline. Therefore this count would have been known in the Fisher system. As to the unknown count (and counter therefore)(claims 1,3,7,8,14,18) Fisher uses the number of speculatively issued instructions that produce a cache hit. This number is not always the same. Therefore this would have been unknown from one execution cycle to the next. This number of

speculatively issued instruction also is indicative of the number of speculatively issued instructions that produced a cache miss since the system would have known how many speculative instructions were issued and the number of speculative instructions issued minus the number of instructions number of speculative instructions that produced a cache hit would have yielded the number of instructions that produced a cache miss. Consequently the counters in Fisher determined a known count and an unknown count that provided data equivalent to the claimed number of command and number of commands in the queue that are used by stall logic.

4. As per claim 4,9,15,19 Fisher taught computing the sum of a known count of instruction and an unknown count of speculatively executed instruction. The sum is compared to a number representative of the number of slots in the command queue to determine whether to stall performance of issued commands (e.g., see col. 9,line 11-col. 10, line 46).

5. As per claims 5,6,10,11 Fisher taught a tracking pipeline that monitors the progress of a plurality of commands and stall request to at least provide a control signal (437) and incrementer (add block 425 in fig. 13) and decrementer (subtract block419) in fig. 13,)(e.g., see figs. 13,14 and col. 14, lines 46-65 and col. 11, lines 5-28).

***Claim Rejections - 35 USC § 103***

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 2,13,17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Fischer (patent No. 6,542,987).

8. As per claim 2, Fisher taught fetch logic (fetch stage in fig. 1); issue logic (100)(e.g., see fig. 2) and execution logic (e.g., see figs. 1,2).

9. Fisher did not expressly detail decode logic. However in order to allow for the use of high level instructions in the Fisher processor one of ordinary skill would have used a decoder to decode the instruction to provide the instructions in a form to be executed.

10. Fisher did not expressly detail claims 13,17, that the stall command comprises receiving a completion signal when stored commands are performed. However in a processors that speculatively executes instructions including loading and storing instructions that would have initiated a stall when a miss was encountered. This would have been done at least to retrieve the requested data in the slower access memory. In that situation as was well known in the art at the time of the claimed invention the stall would last until the memory access was completed and a signal was issued to indicate the completion. This would ensure that data hazards with the load or store would be resolved. Therefore one of ordinary skill would have been motivated to issue a completion signal after a stall was initiated to signal the completion of the stall period.

***Conclusion***

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Shenoy (patent No. 5,455,924) disclosed a system for partial execution blocking of instructions following data cache miss (e.g., see abstract).

Creta (patent No. 5,742,831) disclosed a system for maintaining cache coherency during copendency of load and store operations (e.g., see abstract).

Levine (patent No. 5,949,971) disclosed a system for performance monitoring (e.g., see abstract).

Boggs (patent No. 6,877,086) disclosed a system for rescheduling multiple micro-operations in a processor using a replay queue (e.g., see abstract).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Eric Coleman whose telephone number is (571) 272-4163. The examiner can normally be reached on Monday-Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (571) 272-4162. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

ERIC COLEMAN
PRIMARY EXAMINER